Demo: Observing the Impact of Turn-around Time on the Latency of an SDR Link

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Abstract. Turnaround Time (TT) between transmitting and receiving mode (or vice versa) is important for latency in Half Duplex (HD) communication. In this work, the impact of TT of an SDR radio frontend on latency is demonstrated. Furthermore, to reduce the TT, a new approach — radio frequency frontend operates at full duplex mode, but baseband processing at half duplex mode — is implemented, and the impact on TT is compared against a commercial off-the-shelf chip. Experimental results show that our approach has comparable or even lower latency (16%) than the commercial chip, making SDR an attractive candidate for low latency communications and standards.

Keywords: Software-Defined Radio, Turnaround Time, Latency.

1 Problem Statement

Various wireless applications demand specific requirements e.g., data rate, latency, power consumption, etc., leading to different wireless standards. The capability of Software Defined Radio (SDR) to offer direct access of IQ samples instead of decoded packets and bits, makes it increasingly popular among researchers. One possible way to explore the flexibility of an SDR is to support many wireless standards on a single platform. An SDR, which consists of programmable digital baseband processing unit and reconfigurable analog Radio Frequency (RF) unit, can be operated in Time Division Duplex (TDD) mode. However, the observed switching time of Rx to Tx (or vice versa) or Turnaround Time (TT) in common SDR RF frontend makes it inadequate for wireless standards that need stringent TT (e.g., Wi-Fi).

2 Our Solution

In the context of the ORCA [1] project a unique SDR based solution has been implemented on ZYNQ System on Chip (SoC). In this solution, SDR RF frontend operates in full duplex mode, while baseband processing unit runs in half duplex mode. The proposed approach reduces the TT to zero, enabling the SDR to implement any low latency wireless standard. To verify the effect of our approach on latency, an IEEE

802.15.4 compliant transceiver on SDR is compared against the commercial off-the-shelf chip. The comparison results are shown in the Table 1, which indicates that latency performance of our solution is improved by 16% comparing to commercial chip CC2538 [2].

Table 1. Latency comparison of our solution with commercial off-the-shelf radio chip.

	CC2538 (commercial chip)	Our solution (802.15.4 complaint)
Data Rate (Kbps)	250	250
Signal Bandwidth (MHz)	2	2
Round Trip Time (RTT) (PHY level) (ms with 28 bytes in the air)	2.44	2.049

The demo will show the effect of TT on latency by employing both traditional TDD approach and our approach. To this end, a robot with a wireless closed loop control is balanced. We will demonstrate the importance of latency on time critical applications. Fig. 1 illustrates the steps taken to balance the robot.

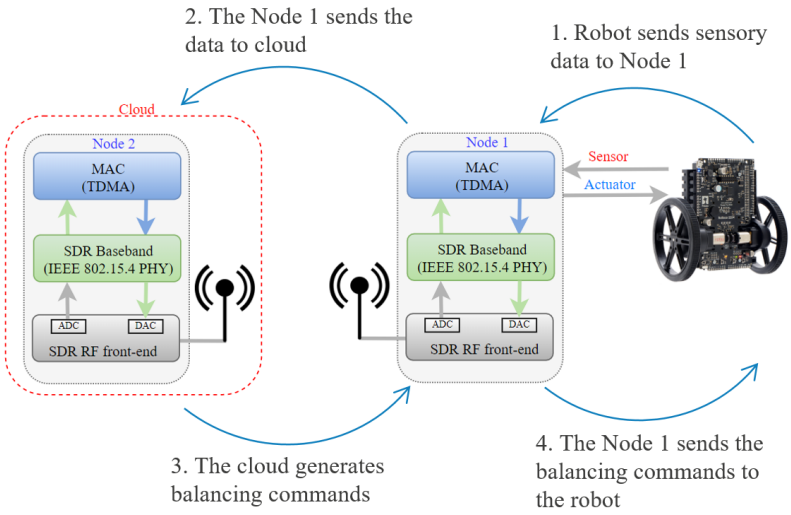

Fig. 1. Wireless closed control loop to balance a robot.

References

1. ORCA (Orchestration Reconfiguration Control Architecture, an EU project in H2020 program) Homepage, https://www.orca-project.eu/, last accessed 2018/06/12.
2. CC2538 datasheet, http://www.ti.com/lit/ds/symlink/cc2538.pdf, last accessed 2018/06/12.